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Assistant Commissioner
For Patents
Washington, D.C. 20231

Attorney Doc. #: 67,200-207
Mailing Date: October 2, 1999

Dear Sir:

Transmitted herewith for filing is the patent application of:

Inventor(s): Ching-Hsing Shih, His-Shen Chuang and Cheng-Fang Chung

For: Apparatus And Method For Cooling A Semiconductor Substrate

Submitted herewith are:

X 3 sheet of informal drawings showing Figs 1-3B

X An Assignment of the invention to Taiwan Semiconductor Manufacturing Co., Ltd., together with Assignment Recordal Sheet

X A Declaration for patent application under CFR 1.63 and 1.68

The filing fee has been calculated as shown below:

	No. Filed	No. Extra	Small Entity Fee	Large Entity Fee	Total
Basic Fee			$380.00	$760.00	$760.00
Total Claims	20x20	5 x	$9.00	$18.00	$0
Indep. Claims	3-3	0 x	$39.00	$78.00	$0
Multiple Dep. Clms.			$130.00	$260.00	$0
Assign. Rec. Fee			$40.00	$40.00	$40.00
TOTAL					$800.00

Mailing Date: October 2, 1999
Attorney Docket No.: 67,200-207

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__X__ Any additional filing fees required under 37 CFR 1.6
__X__ Any patent application processing fees under 37 CFR 1.17

Respectfully submitted,

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Enclosures

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APPARATUS AND METHOD FOR COOLING A SEMICONDUCTOR SUBSTRATE

Field of the Invention

The present invention generally relates to an apparatus and a method for cooling a semiconductor substrate in a process chamber and more particularly, relates to a cooling stage for holding a semiconductor substrate thereon that is provided with a plurality of circular grooves concentrically formed in a top surface of the stage and a plurality of linear grooves formed in radial directions emanating from a center of the top surface in fluid communication with the plurality of circular grooves such that a cooling fluid flows through the grooves to improve cooling of the underside of a substrate placed on the stage and a method for cooling a semiconductor substrate.

Background of the Invention

A frequently used fabrication technique in the manufacture of semiconductor devices involves the deposition of a metallic layer on the surface of a wafer. The deposition process utilizes a thin metal coating to cover steps such as in vias or contact holes that have diameters in the submicron range. The process is essential for achieving precise pattern alignment and reliability in fabricating VLSI and ULSI devices.

Typically, a wafer surface is etched at a plurality of locations which produces a stepped configuration of spaced lines, trenches, vias and contact holes, i.e., the wafer surface is far from being planar. A key requirement of a deposition process is to uniformly and completely fill the

trenches and holes to achieve a generally planar surface. However, the task to completely fill the holes and trenches by using conventional deposition techniques without void formation is very difficult. The presence of voids in a via or contact formed results in poor quality and defective IC devices.

A conventional sputter apparatus that is used to fill trenches or contact holes arranged in a cluster form is shown in Figure 1. The cluster tool 10 consists of four physical vapor deposition chambers 12, 14, 16 and 18 arranged surrounding a transfer chamber 20. On the other end of the cluster tool 10, a number of auxiliary chambers 22, 24, 26 and 28 are arranged surrounding a buffer chamber 30. Further surrounding and in fluid communication with the buffer chamber 30 are the load lock chambers 36 and 38. The buffer chamber 30 and the transfer chamber 20 are both equipped with a wafer transfer robot 32 which is equipped with a robot blade 34. The cluster tool 10 is mounted in a wafer fab facility by through-the-wall installation such that the load lock chambers 36, 38 face the clean room and the process chambers 12~18 are located in a service area. The load lock chambers 36, 38 are used for load and unload wafers into and out of the cluster tool by a machine operator.

Inbetween the buffer chamber 30 and the transfer chamber 20 are positioned two intermediary chambers, i.e., a pre-clean chamber 40 and a cool-down chamber 42. The pre-clean chamber 40 is used for pre-cleaning a wafer before it is delivered to the transfer chamber and subsequently into a sputter chamber. The cool-down chamber 42 is utilized for cooling down a

substrate between a high temperature sputter process and a low temperature sputter process.

A detailed, perspective view of the cool-down chamber 42 is shown in Figure 2. The cool-down chamber 42 may be constructed by a wafer pedestal 44, a chamber base 46, a wafer lifting device 48, a chamber housing 50 which includes a wafer port 52 and a pumping port 54, a wafer lifting ring 58 and a chamber cover 60. As shown in Figure 2, the wafer lifting device 48 operates through the chamber base 46 on the wafer lifting ring 58 for loading and unloading of a wafer (not shown) onto and off the top surface 62 of the wafer pedestal 44. The wafer is first delivered through the wafer port 52 into the chamber housing 50 by a robot blade. The wafer pedestal 44 is cooled by internal cooling channels (not shown) in which a cooling water is circulated through during the operation of the cool-down chamber 42. When a wafer is positioned on the top surface 62 of the wafer pedestal 44, the bottom surface of the wafer is cooled by heat conductance between the wafer and the wafer pedestal 44 while the top surface of the wafer is cooled by a cooling gas circulated through a cavity in the chamber housing 50. The cooling gas circulated through the cavity is normally an inert gas such as argon, nitrogen or helium.

In the cluster tool 10 shown in Figure 1, a semiconductor substrate is frequently processed in several sputter chambers during a multi-layer deposition process. For instance, a frequently used sputtering process involves the deposition of an aluminum/copper alloy on a substrate surface followed by the deposition of an anti-reflective coating (ARC) layer on top by a material such as TiN so that the metal layer can be processed in a subsequent photolithographic

process. The ARC coating layer is important since it avoids a focusing problem that otherwise result from a reflective surface of the aluminum.

In a typical AlCu/TiN process, the processing temperatures used for the two sputtering processes vary to a large extent. For instance, the AlCu deposition may be conducted at a temperature of about 300°C, while the TiN sputtering process may be conducted at a temperature below 200°C. A rapid cool-down process must therefore be conducted to reduce the temperature of the substrate between the two processes. In the operation of the cool-down chamber 42, it has been noticed that the cooling of the bottom side of a substrate is inefficient using a conventional pedestal even though an intimate contact is established between a smooth wafer surface and a smooth pedestal surface. The cooling efficiency by heat conductance to the cooling fluid flown through the wafer pedestal does not approach that of the cooling fluid flown through the chamber cavity for cooling the top surface of the wafer. Due to a significant difference existed between the cooling rates on the top surface and on the bottom surface of the wafer, thermal stresses produced by the temperature difference are also significantly different in the top surface and in the bottom surface of the wafer. Since wafers are very thin, a large difference in the thermal stresses existed between the two surfaces frequently cause a vertical movement of the wafer from the pedestal surface, i.e., the wafer jumps up from the pedestal surface to at least 1 cm. Whenever the wafer jump occurs, the position of the wafer is changed on the pedestal and thus the loading of the wafer by the wafer lifting ring 58 is dislocated. This results in an inaccurate placement of the wafer or more seriously, the dropping of the wafer from the lifting ring resulting in a total loss of the wafer.

Furthermore, the intimate contact between two smooth surfaces of the wafer and the wafer pedestal frequently results in a suction force between the two surfaces. The suction force prevents the wafer from being picked up by the wafer lifting ring 58 and thus cause further processing difficulties.

It is therefore an object of the present invention to provide a wafer pedestal for cooling a semiconductor substrate positioned thereon that does not have the drawbacks or shortcomings of the conventional wafer pedestals.

It is another object of the present invention to provide a cooling stage for a semiconductor substrate that can be effectively used as a wafer pedestal for improved cooling of a semiconductor substrate.

It is a further object of the present invention to provide a cooling stage for a semiconductor substrate that can be used effectively in cooling a semiconductor substrate without the occurrence of the wafer jump phenomenon.

It is another further object of the present invention to provide a cooling stage for a semiconductor substrate that can be used efficiently for cooling a substrate without creating a suction force between the substrate and the cooling stage.

It is still another object of the present invention to provide a cooling stage for a semiconductor substrate that utilizes a wafer pedestal provided with a grooved surface for achieving improved cooling of the wafer.

It is yet another object of the present invention to provide a cooling stage for a semiconductor substrate wherein a pedestal is equipped with a plurality of circular grooves concentrically formed in a top surface and a plurality of linear grooves formed in radial directions emanating from a center of the top surface.

It is still another further object of the present invention to provide a method for cooling a semiconductor substrate by first providing a cooling stage that includes a wafer pedestal equipped with a grooved top surface, then flowing a cooling gas through the grooves to carry away heat from a backside of a semiconductor substrate positioned on the stage.

It is yet another further object of the present invention to provide a wafer pedestal that is effective in cooling a high temperature processed wafer that includes a pedestal that has a groove surface including at least five circular grooves concentrically formed in the top surface and three linear grooves formed in radial directions emanating from a center of the top surface.

Summary of the Invention

In accordance with the present invention, a cooling stage for a semiconductor substrate and a method for using such cooling stage for the effective cooling of a heated substrate are provided.

In a preferred embodiment, a cooling stage for a semiconductor substrate is provided which includes a pedestal that has a substantially planar top surface, a first plurality of circular grooves concentrically formed in the top surface, and a second plurality of linear grooves formed in radial directions emanating from a center of the top surface in fluid communication with the first plurality of circular grooves allowing a cooling fluid to flow therethrough when the semiconductor substrate is positioned on the top surface of the pedestal.

In the cooling stage for a semiconductor substrate, the first plurality may be at least three and the second plurality may be at least two, or the first plurality may be preferably five and the second plurality may be preferably three. The first plurality of circular grooves and the second plurality of linear grooves each may have a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm, or each may have a width preferably between about 3 mm and about 5 mm, and a depth preferably between about 1 mm and about 3 mm. The cooling stage may be situated in a cool-down chamber in a cluster tool for sputtering of metals on semiconductor wafers. The cooling stage may be used in a cool-down chamber between a high temperature sputtering process and a low temperature sputtering process for cooling down a substrate or a wafer.

The present invention is further directed to a method for cooling a semiconductor substrate that includes the steps of providing a cooling stage that includes a wafer pedestal equipped with a grooved top surface thereon, the grooved top surface includes a first plurality of circular grooves concentrically formed in the top surface and a second plurality of linear grooves formed in radial directions emanating from the center of the top surface in fluid communication with the first plurality of circular grooves, positioning a heated semiconductor substrate on the grooved top surface, flowing a cooling liquid through a cooling channel in the wafer pedestal to carry away heat transferred to the grooved top surface, and flowing a cooling gas through the first and second plurality of circular grooves to carry away heat from a backside of the heated semiconductor substrate.

In the method for cooling a semiconductor substrate, the grooved top surface may further include two linear grooves, and preferably at least five circular grooves and at least three linear grooves. The method may further include the step of providing the grooved top surface with a plurality of circular and linear grooves each having a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm, and preferably a width between about 3 mm and about 5 mm, and a depth between about 1 mm and about 3 mm. The method may further include the step of positioning a semiconductor substrate that exits from a high temperature sputtering chamber on the grooved top surface of the cooling stage. The method may further include the step of removing a cooled-down semiconductor substrate from the cooling stage and positioning the substrate in a low temperature sputtering chamber.

The method may further include the steps of flowing a cooling liquid of cooling water through a cooling channel in the wafer pedestal, and flowing a cooling gas of an inert gas through the first and second plurality of circular and linear grooves.

In another preferred embodiment, a wafer pedestal that is effective in cooling a high temperature processed wafer is provided which includes a wafer pedestal that has a substantially planar top surface, at least three circular grooves concentrically formed in the top surface, and at least two linear grooves formed in radial directions emanating from a center of the top surface in fluid communication with the at least three circular grooves such that a cooling fluid flows through the circular and the linear grooves to cool a wafer positioned thereon.

In the wafer pedestal that is effective in cooling a high temperature processed wafer, the wafer pedestal is positioned in a cooled-down chamber between a high temperature sputtering chamber and a low temperature sputtering chamber. The wafer pedestal preferably includes at least five circular grooves and at least three linear grooves provided in a top surface of the pedestal. The wafer pedestal may further include nine circular grooves and three linear grooves each having a width of about 2 mm and a depth of about 1 mm. The cooling fluid flowing through the circular and the linear grooves is an inert gas selected from the group consisting of argon, nitrogen and helium.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will become apparent from the following detailed description and the appended drawings in which:

Figure 1 is a plane view illustrating a conventional cluster tool for conducting a sputtering process utilizing a cool-down chamber.

Figure 2 is a perspective view of the major components used in a cool-down chamber including a wafer pedestal having a smooth top surface.

Figure 3A is a plane view of the present invention wafer pedestal showing the plurality of circular grooves and the plurality of linear grooves.

Figure 3B is a cross-sectional view of the present invention wafer pedestal showing the depth of the circular grooves.

Detailed Description of the Preferred Embodiment

The present invention discloses a cooling stage for use in cooling a semiconductor substrate and a method for utilizing such cooling stage for improved cooling of a substrate such that an imbalance of thermal stresses between a top surface and a bottom surface can be avoided.

In the present invention novel cooling stage, a substrate pedestal is provided which has a substantially planar top surface, a first plurality of circular grooves concentrically formed in the top surface, and a second plurality of linear grooves formed in radial directions emanating from the center of the top surface in fluid communication with the first plurality of circular grooves to allow a cooling fluid to flow therethrough when a semiconductor substrate is positioned on top of the pedestal.

In the novel cooling stage, the first plurality of circular grooves provided is at least three, and preferably at least five, while the second plurality of grooves provided is at least two, and preferably at least three. The dimensions of the grooves provided may be a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm, preferably a width between about 3 mm and about 5 mm, and a depth between about 1 mm and about 3 mm. The novel cooling stage may be advantageously situated in a cool-down chamber as part of a cluster tool for sputtering metal on a semiconductor wafer. The cooling stage may be advantageously used between a high temperature sputtering process and a low temperature sputtering process for the rapid and uniform cooling of a wafer from a high process temperature, i.e., 300°C which is frequently encountered in the sputtering of an aluminum/copper alloy.

The present invention further discloses a method for cooling a semiconductor wafer which can be carried out by the operating steps of first providing a cooling stage that has a wafer pedestal equipped with a grooved top surface including circular grooves and linear grooves radiating

from a center of the surface, then flowing a cooling liquid through a cooling channel in the wafer pedestal to carry away heat transferred from the wafer to the grooved top surface when a heated wafer is positioned on the surface, and then flowing a cooling fluid such as an inert gas of argon through the second plurality of circular and linear grooves to carry away heat from a backside of the wafer.

Referring now to Figure 3B, wherein a present invention cooling stage (or wafer pedestal) 70 is shown in a plane view. As stated previously, the top surface 72 of the cooling stage 70 is provided with a plurality of circular grooves 74 and a plurality of linear grooves 36. The circular grooves 74 are concentrically formed on the surface 72 in a suitable number such as at least three. A preferred number is at least five grooves, while 11 grooves are shown in Figure 3A for a cooling stage 70 used for a 300 mm diameter wafer. The linear grooves 76 are provided in radial directions emanating from a center 80 of the top surface 72 intersecting the circular grooves 74 and forming a fluid communication thereinbetween. The width and the depth for the circular grooves 74 and the linear grooves 76 are normally the same. For instance, a suitable width for the grooves may be between about 1 mm and about 7 mm, preferably between about 3 mm and about 5 mm. A suitable depth of the grooves may be between about 1 mm and about 7 mm, and preferably between about 1 mm and about 3 mm. In the grooves 74 shown in Figure 3B, the width and the depth of the grooves are approximately the same, i.e., at about 2 mm. The width and depth of the grooves may be suitably selected depending on the total area of the cooling stage and the characteristics of the substrate surface to be cooled. It is therefore recognized that, the dimensions shown in Figure 3B

is merely used for illustration purpose, any other suitable dimensions may be utilized equally advantageously in the present invention apparatus and method.

The present invention novel apparatus of the cooling stage equipped with cooling channels or grooves on a top surface provides a multiplicity of benefits. For instance, the novel apparatus completely eliminates the wafer jump defect observed during cooling of a hot wafer on a smooth surfaced stage. Secondly, the present invention novel apparatus effectively prevents wafer from being sucked on the cooling stage due to a vacuum effect when a wafer is placed on a smooth surfaced cooling stage. The cooling grooves effectively prevent wafer from adhering to the cooling stage and thus avoid unnecessary mechanical stresses on the wafer. Thirdly, the present invention novel cooling stage effectively prevents wafer from sliding on a cooling stage due to an air cushion effect which otherwise causes a dislocation of the wafer on the cooling stage. The present invention novel apparatus and method uniformly cools a wafer (or a semiconductor substrate) on both its top surface and its bottom surface such that an imbalance in thermal stresses can be avoided to avoid a dislocation of the wafer on the cooling stage.

The present invention novel apparatus and method has therefore been amply described in the above descriptions and in the appended drawings of Figures 3A and 3B.

While the present invention has been described in an illustrative manner, it should be understood that the terminology used is intended to be in a nature of words of description rather

than of limitation.

Furthermore, while the present invention has been described in terms of a preferred embodiment, it is to be appreciated that those skilled in the art will readily apply these teachings to other possible variations of the inventions.

The embodiment of the invention in which an exclusive property or privilege is claimed are defined as follows:

Claims

1. A cooling stage for a semiconductor substrate comprising:

a pedestal having a substantially planar top surface,

a first plurality of grooves concentrically formed in said top surface, and

a second plurality of linear grooves formed in radial directions emanating from a center of said top surface in fluid communication with said first plurality of circular grooves allowing a cooling fluid to flow therethrough when said semiconductor substrate is positioned on said top surface of the pedestal.

2. A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality is at least 3 and said second plurality is at least 2.

3. A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality is preferably at least 5 and said second plurality is preferably at least 3.

4. A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality of circular grooves and said second plurality of linear grooves each having a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm.

5. A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality of circular grooves and said second plurality of linear grooves each having a width

preferably between about 3 mm and about 5 mm, and a depth preferably between about 1 mm and about 3 mm.

6. A cooling stage for a semiconductor substrate according to claim 1, wherein said cooling stage being situated in a cool-down chamber in a cluster tool for sputtering of metals on semiconductor wafers.

7. A cooling stage for a semiconductor substrate according to claim 1, wherein said cooling stage being used in a cool-down chamber positioned between a high temperature sputtering process and a low temperature sputtering process for cooling down a wafer.

8. A method for cooling a semiconductor substrate comprising the steps of:

providing a cooling stage comprising a wafer pedestal equipped with a grooved top surface thereon, said grooved top surface comprises a first plurality of circular grooves concentrically formed in said top surface and a second plurality of linear grooves formed in radial directions emanating from a center of said top surface in fluid communication with said first plurality of circular grooves,

positioning a heated semiconductor substrate on said grooved top surface,

flowing a cooling liquid through a cooling channel in said wafer pedestal to carry away hat transferred to said grooved top surface, and

flowing a cooling gas through said first and second plurality of circular and linear grooves to carry away heat from a backside of said heated semiconductor substrate.

9. A method for cooling a semiconductor substrate according to claim 8, wherein said grooved top surface further comprises at least 3 circular grooves and at least 2 linear grooves.

10. A method for cooling a semiconductor substrate according to claim 8, wherein said grooved top surface comprises preferably at least 5 circular grooves and at least 3 linear grooves.

11. A method for cooling a semiconductor substrate according to claim 8 further comprising the step of providing said grooved top surface with a plurality of circular and linear grooves, each having a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm.

12. A method for cooling a semiconductor substrate according to claim 8 further comprising the step of providing said grooved top surface with a plurality of circular and linear grooves, each preferably having a width between about 3 mm and about 5 mm, and a depth of between about 1 mm and about 3 mm.

13. A method for cooling a semiconductor substrate according to claim 8 further

comprising the step of positioning a semiconductor substrate exiting a high temperature sputtering chamber on said grooved top surface of said cooling stage.

14. A method for cooling a semiconductor substrate according to claim 8 further comprising the step of removing a cooled-down semiconductor substrate from said cooling stage and positioning the substrate in a low temperature sputter chamber.

15. A method for cooling a semiconductor substrate according to claim 8 further comprising the steps of flowing a cooling liquid through said cooling channel in said wafer pedestal, and flowing a cooling gas of an inert gas through said first and second plurality of circular and linear grooves.

16. A wafer pedestal effective in cooling a high temperature processed wafer comprising:

a wafer pedestal having a substantially planar top surface,

at least 3 circular grooves concentrically formed in said top surface, and

at least 2 linear grooves formed in radial directions emanating from a center of said top surface in fluid communication with said at least 3 circular grooves such that a cooling fluid flows through said circular and said linear grooves to cool said high temperature processed wafer positioned thereon.

17. A wafer pedestal effective in cooling a high temperature processed wafer according to claim 16, wherein said wafer pedestal being positioned in a cool-down chamber positioned between a high temperature sputter chamber and a low temperature sputter chamber.

18. A wafer pedestal effective in cooling a high temperature processed wafer according to claim 16, wherein said wafer pedestal preferably comprises at least 5 circular grooves and at least 3 linear grooves.

19. A wafer pedestal effective in cooling a high temperature processed wafer according to claim 16 further comprising 9 circular grooves and 3 linear grooves each having a width of about 2 mm and a depth of about 1 mm.

20. A wafer pedestal effective in cooling a high temperature processed wafer according to claim 16, wherein said cooling fluid flown through said circular and said linear grooves is an inert gas selected from the group consisting of argon, nitrogen and helium.

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APPARATUS AND METHOD FOR COOLING A SEMICONDUCTOR SUBSTRATE

Abstract of the Disclosure

A cooling stage for a semiconductor substrate and a method for utilizing such cooling stage for improved cooling of a semiconductor substrate are provided. In the cooling stage, a pedestal that has a substantially planar top surface is equipped with a first plurality of circular grooves concentrically formed in the top surface and a second plurality of linear grooves formed in radial directions emanating from a center of the top surface in fluid communication with the first plurality of circular grooves to allow a cooling fluid to flow therethrough when a semiconductor substrate is positioned on the top surface of the stage. The present invention novel apparatus and method is effective in preventing wafer jump or wafer sticking problems frequently caused by an imbalance of thermal stresses in a top surface and a bottom surface of a wafer that is inadequately cooled on a cooling stage.

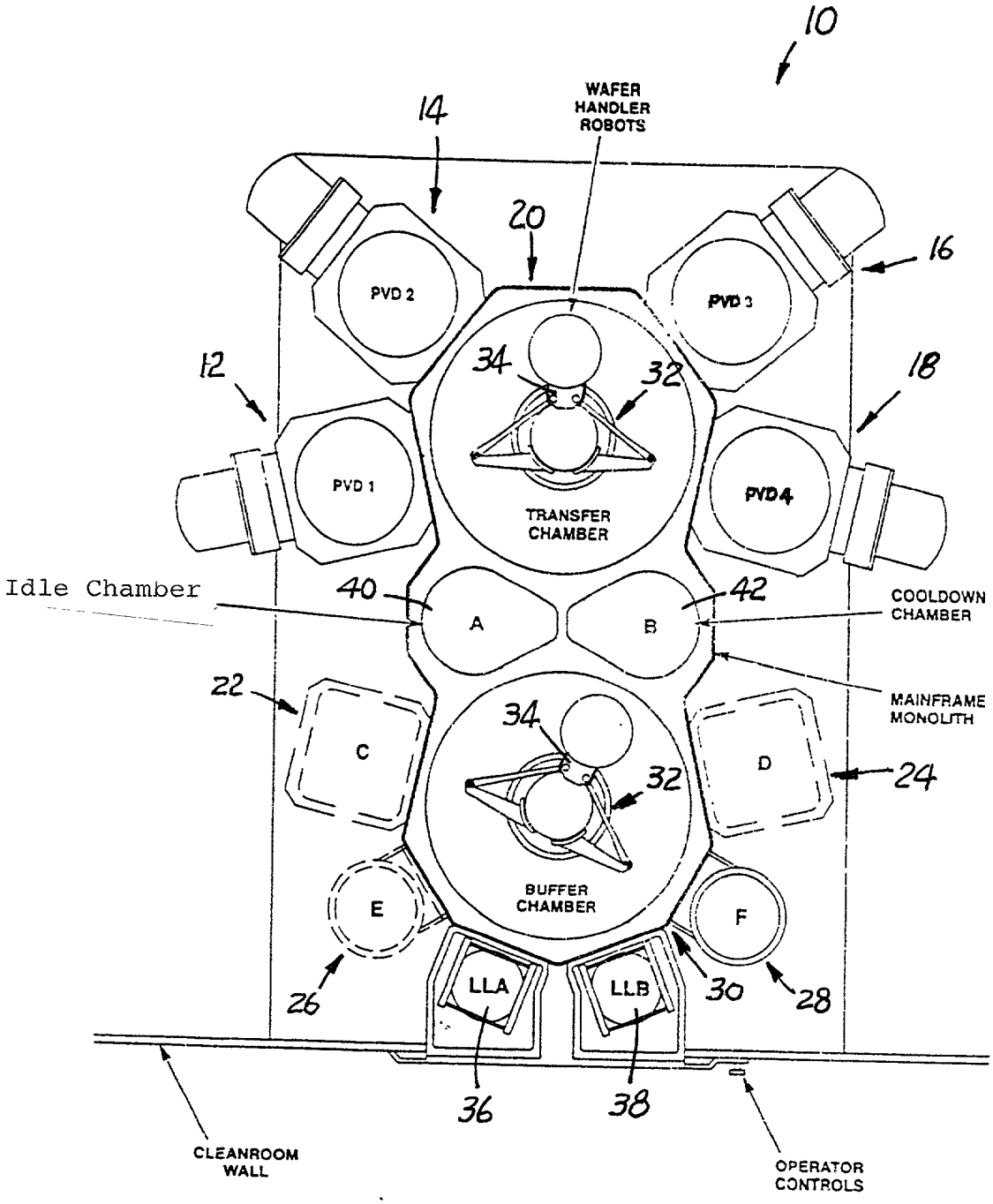

Fig 1.
(Prior Art)

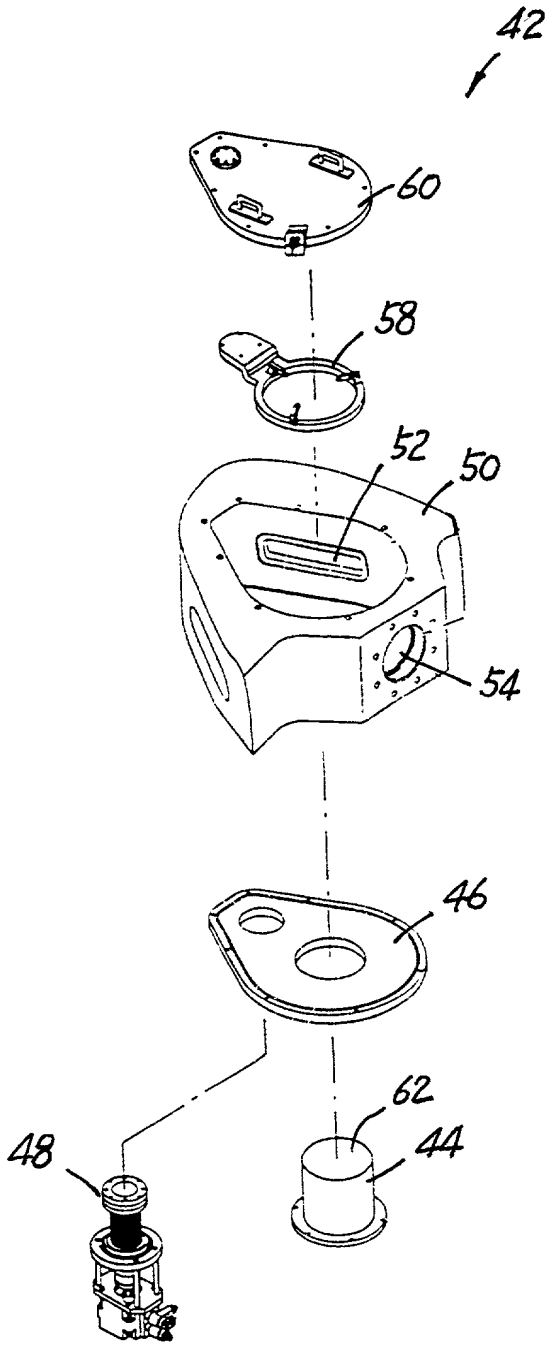

Fig 2.

(Prior Art)

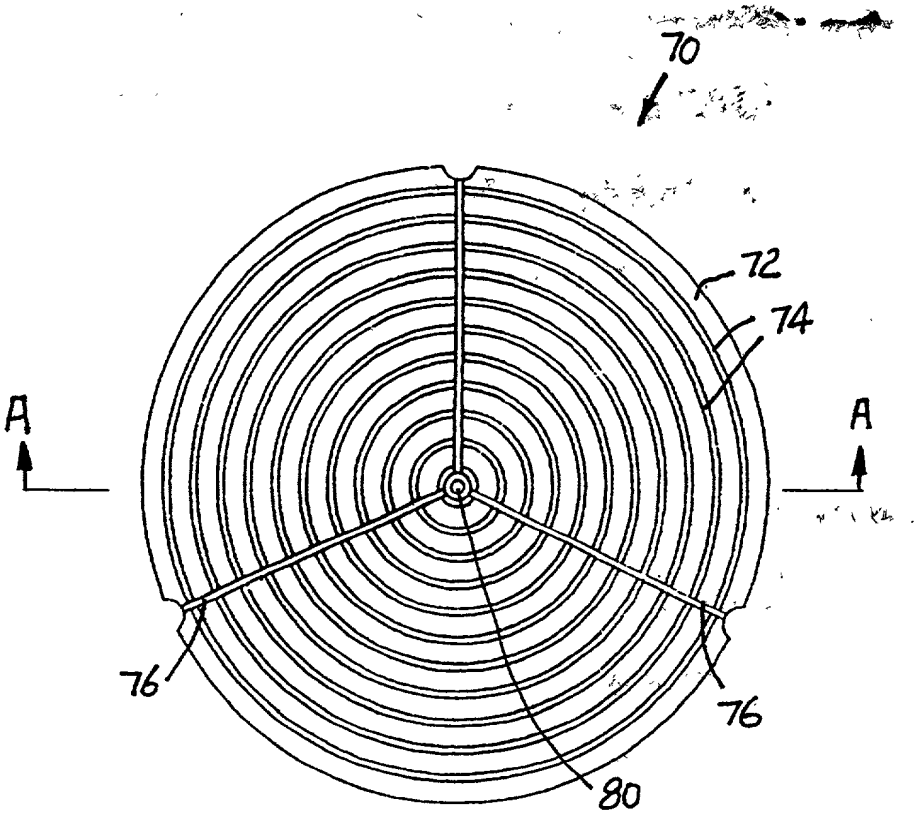

Fig 3A

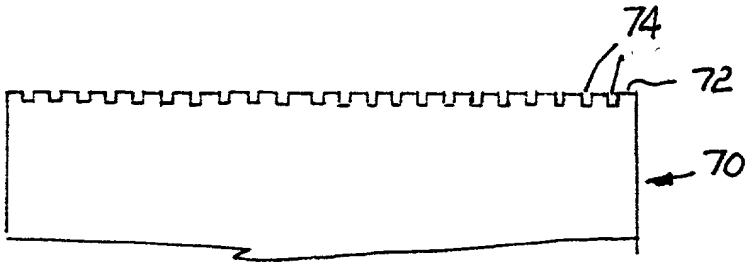

Fig 3B

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DECLARATION FOR PATENT APPLICATION

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "APPARATUS AND METHOD FOR COOLING A SEMICONDUCTOR SUBSTRATE" the specification of which

__X__ is attached hereto.

___ was filed on _____ as
Application Serial No. _____
And was amended on _____
(If applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendments referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56, a copy of which is attached.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application(s) for patent on inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			**Priority Claimed**	
Number	Country	Day/Month/Year	(Yes)	(No)
Number	Country	Day/Month/Year	(Yes)	(No)
Number	Country	Day/Month/Year	(Yes)	(No)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States

application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Ser. No.	Filing Date	Status
Application Ser. No.	Filing Date	Status

I further declare that I do not know and do not believe that the invention claimed in this application was ever known or used by others in this country before my invention thereof, or patented or described in any printed publication in any country before my invention thereof, or more than one year prior to this application or any prior U.S. application above identified in which said invention may have been disclosed, or in public use or on sale in the United States of America for more than one year prior to this application or any prior U.S. application above identified in which said invention may have been disclosed.

POWER OF ATTORNEY

And I hereby appoint as my attorneys with full power of substitution to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith to the firm of **TUNG & ASSOCIATES,** including the following individual attorneys associated with the firm:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application and of any patent issued thereon.

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Full name of fourth joint inventor: _____ (First) _____ (Middle) _____ (Last)

Inventor's Signature: _____

Date: _____

Residence: _____

Citizenship: Republic of China

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§1.56 Duty to disclose information material to patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application; and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent or inventor.

(35 U.S.C. 6, Pub. L. 97-247)

[42 FR 5593. Jan. 28, 1977, as amended at 47 FR 21751, May 19, 1982; 48 FR 2710, Jan. 20, 1983; 49 FR 554, Jan. 4, 1984; 50 FR 5171, Feb. 6, 1985; 53 FR 47808, Nov. 28, 1988, effective Jan. 1, 1989; 57 FR 2034, January 17, 1992, effective March 6, 1992]